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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
ALI, SYED J

ART UNIT	PAPER NUMBER
2127	

DATE MAILED: 03/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/484,549	DYKE ET AL.	
	Examiner	Art Unit	
	Syed J Ali	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *January 18, 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 6 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Specifically, line 1 of claim 6 contains indefinite language comprising grammatical errors that render the claim indefinite.

Claim 14 recites the limitation "The apparatus" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim 14 recites the limitation "the processing of program code" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1 is rejected under 35 U.S.C. 102(a) as being anticipated by Broder et al. (USPN 5,991,808) (hereinafter Broder).

As per claim 1, Broder discloses a method for providing multimedia functionality in a homogeneous multiprocessor environment comprising the steps of:

queuing tasks (col. 5 lines 5-19, "In multiserver systems such as system 100 of FIG. 1, the load data, i.e., the queue loading, for each server changes each time a new task is entered into or leaves the queue of that server", wherein upon allocating tasks for execution at a particular processing unit, the task is added to the queue of that processing unit, which in this case is a server);

identifying available processing resources in the homogeneous multiprocessor environment (col. 5 lines 40-63, "a number of severs selected uniformly at random are queried for load information by the client having a task to be performed", wherein various strategies are employed to determine the available processing resources, and tasks are distributed according to which of those resources is the least loaded);

allocating the available processing resources among the tasks (col. 5 line 64 – col. 6 line 10, "The client 12 then automatically directs the transmission of the task to the identified least loaded of the servers 60 and 66 for servicing", wherein a task is allocated to the server which is determined to be the least loaded, thus allocating an available processing resource to a task in need of scheduling);

providing to the available processing resources functional programs and initial data corresponding to the tasks (col. 6 lines 11-37, "When the task is at the head of the queue, it is serviced by the server and the appropriate response is directed by the server to the client", wherein the servers disclosed are implemented in such a way as they are capable of executing the task, and thus any functional programs and corresponding data necessary for the servicing of the tasks are assumed to be available);

performing the tasks using the available processing resources to produce resulting data (col. 6 lines 11-37, "When the task is at the head of the queue, it is serviced by the server and the appropriate response is directed by the server to the client", wherein the processing resources performs the task when it has reached its turn in the queue).

3. Claim 13 is rejected under 35 U.S.C. 102(b) as being anticipated by Fitch et al. (USPN 5,526,521) (hereinafter Fitch).

As per claim 13, Fitch discloses an apparatus comprising:

a plurality of processors coupled to a bus (col. 3 lines 38-44, "four processing nodes 12 [or processing stacks] are shown in FIG. 2 to be coupled to a communications interface");

an input/output interface coupled to the bus (col. 3 lines 45-52, "Each control system or kernel 24 inherently understands that it is part of a larger system, i.e., a parallel data processing environment", wherein it is well known that a computer system contains a plurality of I/O devices such as keyboards, mice, monitors, and printers among others, and that each of these has a device interface that allows it to interact with the system through a bus);

a plurality of input/output devices coupled to the input/output interface (see parenthetical reference above), the plurality of processors processing program code configured to perform a plurality of tasks, the program code comprising:

program code configured to cause a first portion of the plurality of processors to interact with a first input/output device of the plurality of input/output devices (col. 3 line 53 – col. 4 line 14, "every processing node 12 in the parallel data processing environment has a single address space", "Operating systems divide the machine environment managed by an operating system among different control contexts", wherein it is possible for the operating system to divide the managing of the machine such that each processing node interacts with a single I/O device);

program code configured to cause a second portion of the plurality of processors to interact with a second input/output device of the plurality of input/output devices (see parenthetical reference above);

program code configured to cause a second portion of the plurality of processors to emulate a specific microprocessor instruction set (col. 4 lines 3-14, "Operating systems divide the machine environment managed by an operating system among different control contexts", wherein multiple contexts may run on a single machine. Specifically, the operating system can divide the managing of the system among the processors, and request that a certain set of the processors execute a specific control context, i.e., instruction set).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-3, 5-11, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Broder in view of Fitch.

As per claim 2, Broder does not specifically disclose the method of claim 1 wherein a plurality of processors of the homogeneous multiprocessor environment are capable of executing a first instruction of a first instruction set and a second instruction of a second instruction set. However, Broder does address that the method disclosed therein could be applied to either a homogeneous or a heterogeneous system (col. 1 lines 60-67). However, the heterogeneous system of Broder is meant to apply to different processor speeds, etc. and not to the execution of multiple instruction sets. However, Fitch discloses a method of scheduling tasks where multiple control contexts may run on a single system (col. 3 lines 44-52, "Each control system or kernel 24 inherently understands that it is part of a larger system, i.e., a parallel data processing environment. The kernels control the flow of information between processing nodes"). While the method of Broder applies to a multiserver environment, the multiple servers can still be considered multiple processing resources. In that sense, the same method can be applied to any multiprocessor environment that is capable of performing the load testing of Broder. Accordingly, Fitch discloses a method that is readily adaptable to any number of scheduling algorithms (fig. 4A, element 50, wherein the scheduling algorithm to be employed could easily be altered to accommodate the functionality desired). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of Broder and Fitch since the method of

Broder lacks the ability to run multiple contexts on a single system while dynamically allocating tasks for execution, and Fitch makes up for this deficiency by providing a system that can employ various scheduling techniques while running multiple contexts.

As per claim 3, neither Broder not Fitch specifically disclose the method of claim 2 wherein the first instruction and the second instruction share an identical bit pattern but perform different operations. However, this is interpreted to be a case where two different operations share an identical bit pattern due to the fact that they are from differing contexts. Specifically, when the operation is translated from source code and eventually is executed by the system as binary code, the binary code may be identical despite the fact that the two instructions are dissimilar. In essence, the scope of the claim applies to the system's ability to distinguish the meaning of an operation based on the context in which it was received. Accordingly, what is disclosed in Fitch applies here, since the method of Fitch allows for multiple contexts to run on a single system. Therefore, the method of Fitch inherently may have two different operations that share an identical bit pattern, as claimed.

As per claim 5, Fitch discloses the method of claim 3 further comprising the step of:

converting a functional program of the functional programs expressed using the first instruction set to an equivalent functional program expressed using the second instruction set (col. 5 lines 40-58, "if a context switch is warranted, then a context switcher is called", wherein the method determines if the currently executing context is the proper one, and if so, executes accordingly, but if a switch is necessary, the context is switched and the program or function

being executed is then serviced in the proper environment. By switching contexts, the program is essentially converted from one instruction set to another).

As per claim 6, Broder and Fitch disclose the method of claim 3 further wherein the tasks comprise:

x86 processing;

graphic image processing;

video processing;

audio processing; and

communication processing.

Specifically, the methods of Broder and Fitch are disclosed in a more general sense, and do not specify the systems for which they should be employed. Rather, they are scalable in the sense that they may be implemented on a number of platforms, certainly one of which may be the x86 standard originally developed by Intel, or its compatibles, such as Cyrix or AMD. In addition, the tasks being scheduled in Broder are not limited in scope to multimedia tasks, but rather are intended to cover any task that a computer may execute, such as an online banking service (col. 6 lines 11-37). Therefore, the multimedia tasks claimed can be considered a subset of what is disclosed in Broder, and thus do not comprise an improvement upon what is taught therein.

As per claim 7, Broder discloses the method of claim 3 further comprising the step of:

receiving the initial data from a first input/output device (col. 11 lines 21-34, "commands for processing tasks are entered via the input interface").

As per claim 8, Broder discloses the method of claim 3 further comprising the step of:

passing the resulting data to a first input/output device (col. 6 lines 11-19, "the appropriate response is directed by the server to the client", wherein the client receives the resulting data of the task after having been serviced).

As per claim 9, Broder discloses the method of claim 8 wherein the step of passing the resulting data to the first input/output device further comprises the step of:

passing the resulting data through an intermediary device, wherein the intermediary device is coupled to the first input/output device and to a second input/output device (fig. 1 element 1, wherein the network connecting the clients and servers may comprise any number of intermediary devices such as routers, switches, and hubs. In that sense, the network that allocates tasks among the servers from the clients is coupled to both a first input/output device [client] and a second input/output device [server]).

As per claim 10, Broder discloses the method of claim 9 wherein the step of passing the resulting data through an intermediary device, wherein the intermediary device is coupled to the first input/output device and to a second input/output device further comprises the step of:

automatically adapting to a reallocation of the available processing resources among the tasks (col. 6 line 63 – col. 7 line 3, wherein when the load information corresponding to a specific server varies as tasks are allocated to it for execution, or as they are serviced).

As per claim 11, Broder discloses the method of claim 8 wherein the step of passing the resulting data to a first input/output device further comprises the step of:

passing the resulting data to a mixed-signal device (fig. 1 element 1, wherein it is interpreted that a mixed-signal device is any device capable of digital to analog conversion or vice versa, and the devices described above that may serve as intermediary devices, such as a routers and switches, are capable of acting as such a digital to analog converter or analog to digital converter).

As per claim 14, it is interpreted for the purposes of this examination that the claim is meant to be dependent on claim 14 rather than claim 8. To that effect, Fitch does not specifically disclose the apparatus of claim 14 further comprising:

kernel program code configured to dynamically allocate the processing of the program code among the plurality of processors. However, as discussed above, Fitch does disclose the use of kernel program code. Further, Broder discloses dynamically allocating processing of program code among a plurality of processors (col. 5 line 64 – col. 6 line 10, "The client 12 then automatically directs the transmission of the task to the identified least loaded of the servers 60 and 66 for servicing", wherein a task is allocated to the server which is determined to be the least loaded, thus allocating an available processing resource to a task in need of scheduling).

Therefore, all of the limitations of claim 14 are met by the combination of Fitch and Broder. Further, the motivation for combining these references can be found above.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Broder in view of Fitch as applied to claims 2-3 above, and further in view of Frankel et al. (USPN 5,283,900) (hereinafter Frankel).

As per claim 4, neither Broder nor Fitch specifically disclose the method of claim 3 wherein a first processor of the plurality of processors executes an input/output kernel program, the input/output kernel program including a first portion expressed using the first instruction set and a second portion expressed using the second instruction set. However, Frankel does disclose a real-time operating system wherein a processor executes an input/output kernel program (col. 2 lines 10-28, "Some of the real-time kernels also provide I/O and communication functions"). However, it is noted that Frankel does not teach that the kernel may execute in multiple contexts, including a first portion expressed using the first instruction set and a second portion expressed using the second instruction set. However, as discussed above in reference to claims 2 and 3, Fitch discloses a method for running multiple contexts. Therefore, it would have been obvious to one of ordinary skill in the art to specify that one of the processors run an input/output kernel program since that would help to maximize the multimedia capabilities of the system. Frankel relates to this, as Frankel states that the "real-time" kernels may provide I/O functions. As is well known in the art, "real time" is generally meant to refer to applications that have a high processor demand, such as multimedia. Thus, to utilize the idea of Frankel of a dedicated I/O

kernel would have improved the method of Fitch by allowing greater efficiency in executing such real-time applications.

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Broder in view of Fitch as applied to claims 1-3 above, and further in view of Hardwick (USPN 6,292,822).

As per claim 12, neither Broder nor Fitch discloses the method of claim 3 wherein the step of allocating the available processing resources among the tasks is dynamically adjusted. However, Hardwick does disclose a method for dynamically balancing the load among processors in a multiprocessor environment (col. 4 lines 24-40, "before invoking a function call, a processor of the parallel computer determines whether the computational cost of the function call exceeds a threshold. If so, it determines whether another processor is available to process the function call. If another processor is available, the processor seeking help ships the arguments of the call to the available processor and receives the results"). It would have been obvious to combine the functionality of Hardwick with Broder and Fitch for the purpose of ensuring that at any one time, the processing load of a particular processing unit does not exceed a certain threshold. For example, if the method of Broder determines that a certain server is the least loaded and allocates a task to that server, it may cease to be the least loaded server. If another server then services some tasks, it may be beneficial to redistribute the tasks as a new server has become least loaded, thus achieving a more even balance across all processing units.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed J Ali whose telephone number is (703) 305-8106. The examiner can normally be reached on Mon-Fri 8-5:30, 1st Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John A Follansbee can be reached on (703) 305-8498. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Syed Ali
March 3, 2003

MAJID BANKHAH
PRIMARY EXAMINER